Amendments to the Claims

This listing of claims will replace all prior versions and listings of claims in this application.

Listing of Claims

1. (currently amended) Circuitry for synthesizing a clock signal of a particular frequency, comprising:

a first memory storing a first byte pattern;

a second memory storing a second byte pattern;

multiplexer circuitry coupled to said first and second memory and operative to select a predetermined sequence comprising ~~a predetermined number~~ at least one of each of said first byte pattern and ~~a predetermined number~~ of said second byte pattern, wherein said multiplexer circuitry receives the contents of said first and second byte patterns in parallel; and

serializer circuitry that receives said predetermined sequence from said multiplexer circuitry and synthesizes said clock signal by converting said predetermined sequence into a serialized sequence of said selected first and second byte patterns.

2. (original) The circuitry of claim 1, wherein said first byte pattern comprises bits selected from the group consisting of logic LOW bits, logic HIGH bits, and a combination of logic LOW and HIGH bits.

3. (original) The circuitry of claim 1, wherein said second pattern comprises bits selected from the group consisting of logic LOW bits, logic HIGH bits, and a combination of logic LOW and HIGH bits.

4. (cancelled)

5. (previously presented) The circuitry of claim 1, wherein said serializer circuitry outputs said serialized sequence according to a serial clocking frequency.

6. (original) The circuitry of claim 5, wherein said predetermined frequency of said clock signal is based on said serial clocking frequency and said serialized sequence.

7. (previously presented) The circuitry of claim 1, further comprising control circuitry coupled to said multiplexer circuitry wherein said multiplexer circuitry is responsive to the output from said control circuitry, said output instructing said multiplexer circuitry to select said first and second patterns according to said predetermined sequence.

8. (original) The circuitry of claim 1, wherein said predetermined sequence is programmable.

9. (original) The circuitry of claim 1, further comprising differential circuitry that converts said serialized sequence into a differential signal.

10. (original) The circuitry of claim 8, wherein said differential signal is transmitted from said circuitry to receiver circuitry over a transmission medium.

11. (previously presented) The circuitry of claim 1 wherein said circuitry is mounted on a programmable logic device.

12. (previously presented) The circuitry of claim 1 wherein said circuitry is included in a digital processing logic device comprising:

processing circuitry; and

memory coupled to the processing circuitry, wherein at least one of the processing circuitry and the memory includes said circuitry.

13. (previously presented) The circuitry of claim 1 wherein said circuitry is included in an integrated circuit.

14. (previously presented) The circuitry of claim 1 wherein said circuitry is mounted on a printed circuit board.

15. (previously presented) The printed circuit board defined in claim 14, further comprising:

a memory mounted on the printed circuit board.

16. (original) The printed circuit board defined in claim 14 further comprising:

processing circuitry mounted on the printed circuit board.

17. (currently amended) A high speed serial communication system, comprising:

transmission circuitry that synthesizes ~~at least one~~ a clock signal having any one of a plurality of [[a]] predetermined ~~frequency~~ frequencies by serializing a predetermined sequence of first and second byte patterns, wherein said circuitry receives the contents of said first and second byte patterns in parallel, the serialization of which generates a serialized sequence that is transmitted to receiver circuitry at a serial clocking frequency, said predetermined frequency of said ~~at least one~~ clock signal being a function of said serial clocking frequency and said serialized sequence.

18. (currently amended) The system of claim 17, wherein said receiver circuitry receives said serialized sequence at said serial clocking frequency and derives said ~~at least one~~ clock signal by monitoring said serialized sequence for bit transitions, wherein the string of logic HIGH and LOW bits occurring between said transitions represent said predetermined frequency of said ~~at least one~~ clock signal.

19. (original) The system of claim 17, wherein said transmission circuitry comprises:

memory that stores said first and second byte patterns;

multiplexer circuitry that selects which one of said first and second byte patterns are to be serialized; and

serializer circuitry that serializes the byte patterns selected by said multiplexer circuitry.

20. (previously presented) The system of claim 19, wherein said transmission circuitry further comprises:

controller circuitry having stored therein said predetermined sequence for instructing said multiplexer circuitry to select said first and second byte patterns according to said predetermined sequence.

21. (original) The system of claim 17, wherein said first and second byte patterns comprise bits selected from the group consisting of logic LOW bits, logic HIGH bits, and a combination of logic LOW and HIGH bits.

22. (currently amended) The system of claims 21, wherein the bit arrangement of said first and second byte patterns are selected based on said predetermined frequency of said ~~at least one~~ clock signal.

23. (original) The system of claim 17, wherein said serialized sequence is transmitted to said receiver circuitry as a differential signal.

24. (original) The system of claim 17, wherein said predetermined frequency is a frequency existing at or below said serial clocking frequency.

25. (original) The system of claim 17, wherein said transmission circuitry synthesizes another clock cycle having a second predetermined frequency by serializing a second predetermined sequence of third and fourth byte patterns.

26. (original) The system of claim 25, wherein said first and second byte patterns are different than said third and forth byte patterns.

27. (currently amended) A method for synthesizing a clock signal of a predetermined frequency, comprising:

providing a serial clocking frequency;

providing a first byte pattern and a second byte pattern, wherein the contents of said first and second byte patterns are received in parallel;

selecting a predetermined sequence of said first and second byte patterns, wherein said sequence comprises a

predetermined number of said first byte pattern and a predetermined number of said second byte pattern; and

serializing said predetermined sequence according to said serial clocking frequency to generate a serialized sequence, said predetermined frequency being a function of said serialized sequence and said serialized clock signal.

28. (original) The method of claim 27, wherein said first and second byte patterns comprise bits selected from the group consisting of logic LOW bits, logic HIGH bits, and a combination of logic LOW and HIGH bits.

29. (original) The method of claim 27, further comprising transmitting said serialized sequence to receiver circuitry.

30. (original) The method of claim 29, wherein said serialized sequence is transmitted as a differential signal.

31. (cancelled)

32. (original) The method of claim 27, wherein said predetermined frequency is a frequency at or below said serial clocking frequency.

33. (original) The method of claim 27, further comprising monitoring said serialized sequence for bit transitions, wherein said transitions represent said predetermined frequency.

34. (original) The method of claim 27, further comprising:

providing a third byte pattern and a fourth byte pattern;

selecting a second sequence of said third and fourth byte patterns;

serializing said second sequence according to said serial clocking frequency to generate a second serialized sequence, said second predetermined frequency being a function of said second serialized sequence and said serialized clock signal.